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EXAMINER	
GUILL, RUSSELL L	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,007	WHEELER ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32 and 35-37* is/are rejected.

7)☒ Claim(s) *33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an Amendment file September 12, 2005. Claims 30 – 37 were added. No claims were cancelled. Claims 1 – 37 are pending. Claims 1 – 37 have been examined. Claims 1 – 32 and 35 - 37 have been rejected. Claims 33 and 34 have been objected to.

2. **The Examiner would like to thank the Applicant for the well-presented response, which assisted in the examination process.**

Continued Examination

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 12, 2005 has been entered.

Response to Remarks

4. As an initial matter, the Examiner reviewed the Applicants' specification and the art of Watkins (U.S. Patent No. 5,220,512), and the Examiner appreciates that the Applicants' invention performs different, and more complex, processing than the invention of Watkins. However, as discussed below, the claim language of the independent claims does not appear to clearly distinguish the Applicants' invention from the invention of Watkins.

5. Further, in order to expedite the examination process, the Examiner would like to draw attention to the additional new rejections of the independent claims 1, 13 and 25 using new art, such that the independent claims 1, 13 and 25 now have two separate rejections each under 35 U.S.C. 102.

6. Further, in order to expedite the future examination process, the Examiner would like to suggest that the Applicant review the following prior art patents that also appear to anticipate the language of the independent claims:

6.1.1. U.S. Patent No. 6,470,478 by Bargh et al.

6.1.2. U.S. Patent No. 6,920,418 by Roesner et al.

6.1.3. U.S. Patent No. 6,978,231 by Williams et al.

7. Finally, upon further review and consideration, the Examiner has included new rejections under 35 U.S.C. § 101.

8. Regarding claim rejections of **claims 1 – 6 and 13 – 18**:

8.1. The Applicant argues that:

8.1.1. Watkins appears to disclose a system which requires a user to add additional components (e.g. state displays, state tables) to a logic design in order to obtain state information about a particular logic design element or schematic component such as flip-flop 302. Watkins does not appear to teach having the schematic components 304, 306 and 308 collecting data about themselves as required by the logic design elements of the invention of claims 1 – 6 and 13 – 18.

8.1.1.1. The Examiner respectfully replies: Under a broad reasonable interpretation, the logic design element appears to automatically collect instrumentation data because:

8.1.1.1.1. the state information (referred to in the previous paragraph) is stored and available independent of the added "state display components", and state information appears to be instrumentation data related to the logic element displayed in Figure 3 of Watkins, and

8.1.1.1.2. the instrumentation data (i.e., state information) is collected automatically during the simulation process, since the value of the state variable is computed during simulation.

8.1.1.2. Accordingly, the rejections are maintained.

9. Regarding claim rejections of **claims 25 - 27**:

9.1. The Applicant argues that:

9.1.1. The ECAD system of Watkins does not teach **a collection module that is integrated with the logic design element** and that is structured and arranged **to automatically collect instrumentation data relating to the logic design element** during the simulation.

9.1.1.1. The Examiner respectfully replies: Under a broad reasonable interpretation, Watkins appears to teach (especially column 7, lines 11 – 27) **a collection module that is integrated with the logic design element** and that is structured and arranged **to automatically collect instrumentation data relating to the logic design element** during the simulation. Under a broad reasonable interpretation of a module, the simulator is a collection module that is integrated

with the logic design element, and automatically collects instrumentation data relating to the logic design element.

9.1.1.2. Accordingly, the rejections are maintained.

10. Regarding claim rejections under 35 USC § 103, **claims 7 – 9, 19 – 21, and 28 (Watkins/Sharma)**:

10.1. The Applicant argues specifically that:

10.1.1. The art of Sharma teaches away from simulation techniques.

10.1.1.1. The Examiner respectfully replies: Sharma teaches known prior art problems with both simulation and emulation, but only to show the benefit of his invention by comparison. Without in any way conceding the validity of the Applicants' argument, in order to expedite the examination process, the Examiner is modifying the motivation to use the art of Sharma to be the benefits recited in Sharma that his invention reduces the number of bugs, particularly the queue flow control bugs, early in the design flow that results in a superior system design potentially a faster tune to market (column 3, lines 1 – 10).

11. Regarding claim rejections under 35 USC § 103, **claims 10 - 12, 22 – 24, and 29**:

11.1. The Applicant argues specifically that:

11.1.1. The claims are allowable for at least the reasons given for claims 1, 13 and 25.

11.1.1.1. The Examiner respectfully replies: Please refer to the Examiner's reply to the arguments for claims 1, 13 and 25.

Claim Rejections - 35 USC § 101

12. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

13. Claims 1, 7 - 8, 10 - 11, 25 - 29, 30 - 31 and 35 - 37 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. Regarding **claims 1, 7 - 8, 10 - 11 and 30 - 31**, the claims do not appear to produce a useful and tangible result to form the basis of a practical application needed to be statutory.

b. Regarding **claims 25 - 29 and 35 - 37**, the claims appear to be directed to an arrangement of software and data being claimed as a set of functional and non-functional descriptive material per se, and as such, is non-statutory.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an

application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15. (**NEW REJECTION**) Claims 1, 13 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Bargh (U.S. Patent 6,195,627).

15.1. Regarding **claims 1 and 13**:

15.1.1. Bargh appears to teach a method and machine-accessible medium using a logic design element in a logic design (***Abstract***).

15.1.2. Bargh appears to teach a method and machine-accessible medium performing a simulation of the logic design that includes simulating the logic design element (***Abstract***).

15.1.3. Bargh appears to teach a method and machine-accessible medium having the logic design element automatically collect instrumentation data during the simulation, wherein the instrumentation data relate to the logic design element (***figures 4A and 4B; and column 12, lines 25 – 67, and columns 13 – 14; please note that in figure 4B, element TOP:TOP is also a logic design entity, as discussed in columns 7 - 8***).

15.2. Regarding **claim 25**:

15.2.1. Bargh appears to teach a simulation module that is structured and arranged to perform a simulation of a logic design that includes a logic design element (***Abstarct, and columns 7 – 8, and figures 3A and 3B***).

15.2.2. Bargh appears to teach a collection module that is integrated with the logic design element and that is structured and arranged to automatically collect

instrumentation data relating to the logic design element during the simulation (***figure 4B, element 420; and column 12, lines 25 – 67, and columns 13 – 14***).

16. Claims 1 – 6 and 13 - 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins (U.S. Patent 5,220,512).

16.1. Regarding claims 1 and 13:

16.1.1. Watkins appears to teach a method and machine-accessible medium using a logic design element in a logic design (***figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

16.1.2. Watkins appears to teach a method and machine-accessible medium performing a simulation of the logic design that includes simulating the logic design element (***figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

16.1.3. Watkins appears to teach a method and machine-accessible medium having the logic design element automatically collect instrumentation data during the simulation, wherein the instrumentation data relate to the logic design element (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 - 49***).

16.2. Regarding claims 2 and 14:

16.2.1. Watkins appears to teach displaying the instrumentation data relating to the logic design element (***Figure 3***).

16.3. Regarding claims 3 and 15:

16.3.1. Watkins appears to teach receiving a query to display the instrumentation data relating to the logic design element, wherein displaying the instrumentation data relating to the logic design element in response to the query (***column 6, lines 45 – 53***).

16.3.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

16.4. Regarding claims 4 and 16:

16.4.1. Watkins appears to teach displaying the instrumentation data after performing the simulation (***column 5, lines 14 – 16***).

16.5. Regarding claims 5 and 17:

16.5.1. Watkins appears to teach displaying the instrumentation data while performing the simulation (***column 7, lines 48 – 57***).

16.6. Regarding claims 6 and 18:

16.6.1. Watkins appears to teach performing the simulation means performing a partial simulation (***column 7, lines 12 – 27***).

16.6.2. Watkins appears to teach having the logic design element automatically collect the instrumentation data during the partial simulation (***column 7, lines 24 – 27***).

16.6.3. Watkins appears to teach displaying the instrumentation data includes displaying the instrumentation data after performing the partial simulation (***column 7, lines 12 – 27***).

17. Claims 25 - 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins (U.S. Patent 5,220,512).

17.1. Regarding claim 25:

17.1.1. Watkins appears to teach a simulation module that is structured and arranged to perform a simulation of a logic design that includes a logic design element (***figure 2, element 224; figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

17.1.1.1. Regarding (***figure 2, element 224; figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***); figure 2, element 224, is a simulation module.

17.1.2. Watkins appears to teach a collection module that is integrated with the logic design element and that is structured and arranged to automatically collect instrumentation data relating to the logic design element during the simulation (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 – 49; and column 7, lines 12 - 27***).

17.1.2.1. Regarding (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 – 49; and column 7, lines 12 - 27***); Watkins teaches software that collects data, therefore it would have been inherent that the software has a portion of code to collect data, which is a collection module.

17.2. Regarding claim 26:

17.2.1. Watkins appears to teach a display module that is structured and arranged to display the instrumentation data relating to the logic element design (***column 7, lines 12 – 19; and figure 3; and figure 2, element 224***).

17.2.1.1. Regarding (***column 7, lines 12 – 19; and figure 3; and figure 2, element 224***); Column 7, lines 12 – 19, recites that the simulation module displays the instrumentation data; therefore the logic simulator (***figure 2, element 224***) is a display module.

17.3. Regarding claim 27:

17.3.1. Watkins appears to teach an interface module that is structured and arranged to receive a query to display the instrumentation data relating to the design element, wherein the display module is structured and arranged to display the instrumentation data relating to the logic design element in response to the query (***column 6, lines 45 – 53***).

17.3.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query. Watkins teaches software to receive a query, therefore it is inherent that there is a portion of code that receives the query, which is an interface module to receive the query.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

20. Claims 7 – 9 and 19 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins as applied to claims 1 – 6 and 13 – 18 above, in view of Sharma (U.S. Patent 5,978,574).

20.1. Watkins teaches a method and machine-accessible media of a logic design element that automatically collects instrumentation data as recited in claims 1 – 6 and 13 – 18 above.

20.2. Claim 7 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

20.3. Claim 19 is a dependent claim of claim 13, and thereby inherits all of the rejected limitations of claim 13.

20.4. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

20.5. The art of Sharma is directed to verification of queue flow control through model checking (***Title***).

20.6. Regarding claims 7 and 19:

20.6.1. Watkins appears to teach having the logic design element automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the logic element (***figure 3; and column 5, lines 5 – 10, especially***

"points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 - 4).

20.6.2. Watkins does not specifically teach that ***the logic design element includes a FIFO memory***, and having the logic design element automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the ***FIFO memory***.

20.6.3. Sharma appears to teach that the logic design element includes a FIFO memory (***figure 2; and column 1, lines 63 – 67***).

20.6.4. The motivation to use the art of Sharma with the art of Watkins is the benefits recited in Sharma that the invention reduces the number of bugs, particularly the queue flow control bugs, early in the design flow that results in a superior system design (and a) potentially a faster tune (time) to market (**column 3, lines 1 – 10**).

20.7. Regarding claims 8 and 20:

20.7.1. Watkins appears to teach having the logic elements record usage during the simulation (***figure 4; and column 5, lines 5 – 10; and column 6, lines 45 – 52; and column 7, lines 32 – 35***).

20.7.2. Watkins does not specifically teach having the ***FIFO memory*** record usage ***of the FIFO memory*** during the simulation.

20.7.3. Sharma appears to teach a FIFO memory simulation (***figure 2; and column 2, lines 10 – 13; and column 1, lines 31 – 35***).

20.8. Regarding claims 9 and 21:

20.8.1. Watkins appears to teach receiving a query to display the instrumentation data relating to a logic element (***column 6, lines 45 – 53***).

20.8.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

20.8.2. Watkins appears to teach displaying the instrumentation data relating to the logic element in response to the query (***column 7, lines 36 – 45***).

20.8.3. Watkins does not specifically teach receiving a query to display the instrumentation data relating to the ***FIFO memory***.

20.8.4. Watkins does not specifically teach displaying the instrumentation data relating to ***the FIFO memory*** in response to the query.

20.8.5. Sharma appears to teach a FIFO memory (***figure 2; and column 1, lines 63 – 67***).

20.9. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Sharma with the art of Watkins to produce the claimed invention.

21. Claims 10 - 12 and 22 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins as applied to claims 1 – 6 and 13 – 18 above, in view of Mitchell (U.S. Patent 5,646,553).

21.1. Watkins teaches a method and machine-accessible media of a logic design element that automatically collects instrumentation data as recited in claims 1 – 6 and 13 – 18 above.

21.2. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

21.3. The art of Mitchell is directed toward a driver for a tri-state bus (***Title***).

21.4. Regarding claims 10 and 22:

21.4.1. Watkins appears to teach that having the logic element automatically collect the instrumentation data includes having the logic element automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the logic element (***column 7, lines 12 – 17***).

21.4.2. Watkins does not specifically teach that ***the logic design element includes a tri-state bus***.

21.4.3. Watkins does not specifically teach having the logic element automatically collect the instrumentation data includes having the ***tri-state bus*** automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the ***tri-state bus***.

21.4.4. Mitchell appears to teach that a logic design includes a tri-state bus (***Abstract, and figure 1***).

21.4.5. The motivation to use the art of Mitchell with the art of Watkins is the benefit recited in Mitchell that the circuit avoids contention on the bus by shutting off each device's output enable early, so that it is guaranteed to no longer drive the line by the time any other device begins to drive, while holding the data on the bus until the end of the transfer cycle (***column 1, lines 45 – 50***).

21.5. Regarding claims 11 and 23:

21.5.1. Watkins appears to teach that having a logic element automatically collect the instrumentation data includes having a logic element automatically collect usage of a logic element during the simulation (***column 7, lines 11 – 26; column 6, lines 45 – 53***).

21.5.2. Watkins does not specifically teach that having the ***tri-state bus*** automatically collect the instrumentation data includes having the ***tri-state bus*** automatically collect usage of the ***tri-state bus*** during the simulation.

21.5.3. Mitchell appears to teach a logic design that includes a tri-state bus (***Abstract, and figure 1***).

21.6. Regarding claims 12 and 24:

21.6.1. Watkins appears to teach receiving a query to display the instrumentation data relating to a logic element (***column 6, lines 45 – 53***).

21.6.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

21.6.2. Watkins appears to teach displaying the instrumentation data relating to a logic element in response to the query (***column 7, lines 36 – 45***).

21.6.3. Watkins does not specifically teach receiving a query to display the instrumentation data relating to the ***tri-state bus***.

21.6.4. Watkins does not specifically teach displaying the instrumentation data relating to the ***tri-state bus*** in response to the query.

21.6.5. Mitchell appears to teach a logic design that includes a tri-state bus (***Abstract, and figure 1***).

22. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins as applied to claims 25 - 27 above, in view of Sharma (U.S. Patent 5,978,574).

22.1. Watkins teaches an apparatus of a logic design element that automatically collects instrumentation data as recited in claims 25 - 27 above.

22.2. Claim 28 is a dependent claim of claim 25, and thereby inherits all of the rejected limitations of claim 25.

22.3. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

22.4. The art of Sharma is directed to verification of queue flow control through model checking (***Title***).

22.5. Regarding claim 28:

22.5.1. Watkins appears to teach that the collection module is integrated with the logic design element and is structured and arranged to automatically collect the instrumentation data relating to the logic element during the simulation (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 - 4***).

22.5.2. Watkins does not specifically teach that the collection module is integrated with the ***FIFO memory*** and is structured and arranged to automatically collect the instrumentation data relating to the ***FIFO memory*** during the simulation.

22.5.3. Sharma appears to teach that the logic design element includes a FIFO memory (***figure 2; and column 1, lines 63 – 67***).

22.5.4. The motivation to use the art of Sharma with the art of Watkins is the statement recited in Sharma that verification of queue flow control is traditionally performed through simulation (***column 2, lines 10 – 14; and column 2, lines 31 – 36***).

23. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins as applied to claims 25 – 27 above, in view of Mitchell (U.S. Patent 5,646,553).

23.1. Watkins teaches an apparatus of a logic design element that automatically collects instrumentation data as recited in claims 25 - 27 above.

23.2. Claim 29 is a dependent claim of claim 25, and thereby inherits all of the rejected limitations of claim 25.

23.3. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

23.4. The art of Mitchell is directed toward a driver for a tri-state bus (***Title***).

23.5. Regarding claim 29:

23.5.1. Watkins appears to teach that the collection module is integrated with the logic element and is structured and arranged to automatically collect the instrumentation data relating to the logic element during the simulation (***column 7, lines 12 – 17***).

23.5.2. Watkins does not specifically teach that ***the logic design element includes a tri-state bus***.

23.5.3. Watkins does not specifically teach that the collection module is integrated with the ***tri-state bus*** and is structured and arranged to automatically collect the instrumentation data relating to the ***tri-state bus*** during the simulation.

23.5.4. Mitchell appears to teach that a logic design element includes a tri-state bus (***Abstract, and figure 1***).

23.5.5. The motivation to use the art of Mitchell with the art of Watkins is the benefit recited in Mitchell that the circuit avoids contention on the bus by shutting off each device's output enable early, so that it is guaranteed to no longer drive the line by

the time any other device begins to drive, while holding the data on the bus until the end of the transfer cycle (***column 1, lines 45 – 50***).

24. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins as applied to claims 1 – 6 and 13 – 18 above, in view of Wong (K.F. Wong et al.; "Statistics on Logic Simulation", 1986, IEEE 23rd Design Automation Conference).

24.1. Watkins teaches a method and machine-accessible media of a logic design element that automatically collects instrumentation data as recited in claims 1 – 6 and 13 – 18 above.

24.2. Watkins does not specifically teach:

24.2.1. the logic design element represents a FIFO memory;

24.2.2. the instrumentation data collected by the logic design element comprises a degree of fullness of the FIFO memory.

24.3. Wong appears to teach:

24.3.1. the logic design element represents a FIFO memory (**pages 16 – 17, section 5.3 Event Queue Length Distribution**);

24.3.2. the instrumentation data collected by the logic design element comprises statistics regarding usage of the FIFO memory (**page 18, figure 1**).

24.4. The motivation to use the art of Wong with the art of Watkins would have been the benefit recited in Wong that the invention obtains and presents data on the logic simulation process that is important in designing event list scheduling algorithms and hardware (**page**

13, right-side column, fist paragraph). This feature would have been recognized by the ordinary artisan as a benefit to produce higher quality designs.

24.5. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Wong with the art of Watkins to produce the claimed invention.

25. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins as applied to claims 1 – 6 and 13 – 18 above, in view of Srivastava (Mani B. Srivastava et al.;"Using VHDL for High-Level, Mixed-Mode System Simulation", September 1992, IEEE Design & Test of Computers, Volume 9, Issue 3).

25.1. Watkins teaches a method and machine-accessible media of a logic design element that automatically collects instrumentation data as recited in claims 1 – 6 and 13 – 18 above.

25.2. Watkins does not specifically teach:

25.2.1. the logic design element represents a FIFO memory;

25.2.2. the instrumentation data collected by the logic design element comprises statistics regarding usage of the FIFO memory.

25.3. Srivastava appears to teach:

25.3.1. the logic design element represents a FIFO memory (**page 36, figure 3; and page 35, section VHDL model-simulating package**);

25.3.2. the instrumentation data collected by the logic design element comprises statistics regarding usage of the FIFO memory (**page 36, figure 3, message buffer and statistics**).

25.4. The motivation to use the art of Srivastava with the art of Watkins would have been advantages specifically recited in Srivastava that VHDL enables simulation across many different levels of abstraction (**page 31, last sentence, and page 32 first two sentences**), and its process oriented viewpoint makes the expression of concurrence elegant. These advantages would have been recognized by the ordinary artisan as benefits.

25.5. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Srivastava with the art of Watkins to produce the claimed invention.

26. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Allowable Subject Matter

27. Claims 33 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:00 AM – 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

Paul L. Rodriguez
Primary Examiner
Art Unit 2125 ~~2125~~ 2123
Signed 4/13/06